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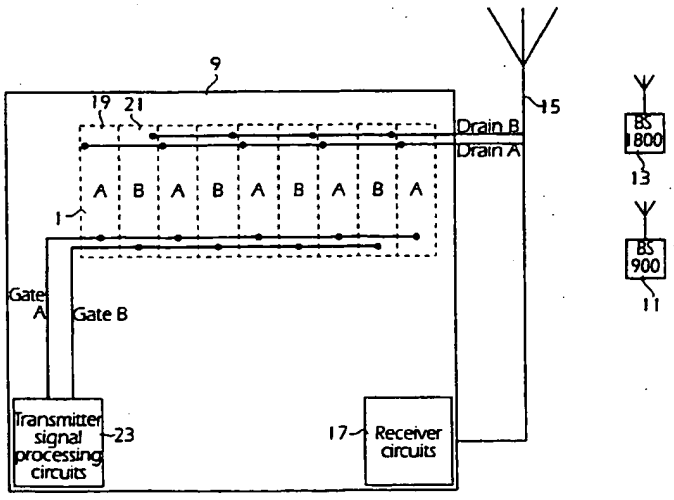
(54) Title: IMPROVED HEAT DISSIPATION IN AN AMPLIFIER CIRCUIT BY INTERLEAVED CONFIGURATION OF TWO POWER TRANSISTORS



(57) Abstract: In an output stage of an electronic signal processing circuit such as that used for transmission from a mobile telephone set the amplifier circuit comprises two power transistors (A, B) of type FET. The power transistors are used for amplifying different signals such as signals for different wavelength bands in a dual band telephone set and they are not used simultaneously. Each power transistor comprises a multitude of elementary transistors (19, 21) or "fingers" which are interdigitated to form an interleaved configuration, the element transistors of one transistor alternating with the element transistors of the other transistor. Thereby the effective area which can receive heat dissipated by the element transistors will be twice that used when the element transistors are located in two geometrically separated groups which will allow a higher power load on each transistor element.

WO 01/24271 A1

Improved heat dissipation in an amplifier circuit by interleaved configuration of two power transistors

TECHNICAL FIELD

The invention is related to an amplifier circuit suitable for amplifying at least two different signals such as signals of two different wavelength bands.

BACKGROUND

In communication with mobile stations there nowadays is a need for using different standards which can require modulation methods suited for the respective amplification methods and hence different amplifier designs can be required. Also different wavelength bands are used in the different standards. In a dual band mobile station the station can receive and transmit signals in two different wavelength bands, e.g. using GSM at wavelengths at 1800 MHz and AMPS at 800 MHz.

In a mobile station such as a mobile telephone set a power amplifier is used in the final step of transmitting signals from the station. In the power amplifier power transistors are used for amplifying the signals. These transistors usually comprise FETs (Field Effect Transistors) of various designs. The output power required for different standards may be different for the respective wavelength bands and thus the output FETs must be driven to produce an output power which is different for each band. For instance, for 900 MHz an output power of 3.5 W can be required and for 1800 MHz the required output power can be 1.6 W. There exists a multitude of standards using different wavelength band such as AMPS for 800 MHz as mentioned above, GSM for 900 and 1800 MHz and PCS for 1900 MHz. Also, the output transistors may have to be designed differently for different standards owing to the use of different modulation methods which require specially selected operating points, etc.

FETs used as output amplifiers can only be designed to optimally produce an output power for a particular small range of the output power. In Fig. 1 a diagram of the efficiency η of a FET is plotted as a function of the output power for some special assumptions which can e.g. include constant drain-source voltage, constant load resistance, only the average gate-source being varied, etc. In the diagram Fig. 1 two graphs are plotted, one for the efficiency of FET optimized for the output power for transmitting at 900 MHz according to some standard and another one for transmitting at 1800 MHz according to some similar standard, which however requires a lower output power. The respective transistors can only be used in the regions lower than the respective shaded area. Suitable operating points are indicated by the dashed lines. It is observed in the figure that a FET designed to optimally work to provide the power required at 900 MHz will have a lower efficiency when used for providing a lower output power at a higher frequency such as 1800 MHz under these assumptions. Generally, thus it is concluded that it is difficult to design an optimized single output FET for a multimode power amplifier. In the example of Fig. 1 different FETs should used which are designed to optimally provide the required output power at the two frequencies. The two FETs could then e.g. each have

as small an area as possible to be suited to provide the respective output power.

However, also the power consumption and the cooling of the FETs must be considered. There is generally an increasing demand for transmitting data from the mobile stations using standard networks. In such networks the time for communicating with a considered base station is divided in time slots so that transmission from a considered mobile station can be made say at most every eighth time slot. This means that if a FET is designed for a particular output power, the power consumption and the power dissipation will only correspond to about an eighth of the amounts required for a continuous transmission. When data transmission is required, more time slots can be assigned to the mobile station, e.g. two or three time slots out of a set of totally eight time slots. This in turn implies that the power amplifiers and the FETs comprised therein must be designed for this higher average output power and thus the cooling of the power circuits has to be improved. This would generally require that the area of the FETs had to be considerably increased in order to enhance the conduction of heat away from the transistors.

In U.S. patents 4,276,516 and 4,682,197 interdigitated bipolar transistor structures for power amplifiers of Class B are disclosed in which neighbouring fingers comprise the complementary transistors which conventionally are alternatingly switched on in such amplifiers.

SUMMARY OF THE INVENTION

It is an object of the invention to provide an amplifier circuit for two different wavelength bands which has an efficient cooling and an efficient use of chip area.

The problem to be solved by the invention is thus how to integrate the different transistors needed for amplifying signals of two wavelength bands in order to occupy a small area on a semiconductor chip and to have transistors located so that the power dissipated by the transistors can efficiently be conducted away.

In a structure of power field effect transistors and for instance used in an output stage of signal processing circuit each individual transistor comprises a multitude of "fingers", the fingers being element or elementary transistors located to form a line or row. By interdigitating the fingers so that element transistors belonging to one power transistor alternate with transistors belonging to another power transistor each element transistor will have a large surface area of a chip which will receive the heat developed by the element transistor. This presupposes that at each instant only one power transistor is active which is true for instance when communicating using different wavelength bands and each wavelength band has its own power transistor.

The element transistors are thus collected in groups to form field effect transistor units which are used for different purposes. One transistor unit can thus be intended for amplifying signals of wavelengths or of wavelength band requiring more electric output power such as a lower frequency band. Since this transistor unit has to supply an output signal having a large output power, it hence requires a large area of a chip. Another

transistor unit can require a smaller area since when it is active less heat is developed, such a transistor unit for instance being intended to amplify signals of a higher frequency. The number of element transistors of a first transistor unit can thus be larger than the number of element transistors of a second transistor unit. Alternatively or combined therewith the element transistors of the second transistor unit can each one occupy a smaller area than the element transistors of the second transistor unit.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described by way of a non limiting embodiment with reference to the accompanying drawings, in which:

- Fig. 1 is a diagram of the efficiency of a power field-effect transistor (FET) as a function of output power,
- Fig. 2a is a schematic view from above of the layout of a single FET finger,
- Fig. 2b is the circuit symbol of a FET,
- Fig. 3 is a schematic view illustrating the use of different output FETs for different communication channels in a mobile unit communication system,
- Fig. 4 is a schematic view similar to that of Fig. 3 illustrating interdigitated elementary FETs,
- Fig. 5a is a schematic view similar to that of Fig. 2a illustrating the layout of the FETs in the embodiment of Fig. 3 and the juxtaposition of FET fingers having sources and drains in common,
- Fig. 5b is a schematic view similar to that of Fig. 5a illustrating a layout of the FETs allowing a heavier load,
- Fig. 5c is a schematic view similar to that of Fig. 5a illustrating a layout of FETs allowing a heavier load and requiring a minimum of space,
- Fig. 6a is a schematic view similar to that of Fig. 5a illustrating an alternative layout of FETs allowing a heavier load and requiring a minimum of space,
- Fig. 6b is the circuit diagram equivalent with the FETs illustrated in Fig. 6a,
- Fig. 7 is a view similar to that of Fig. 3 of another structure of interdigitated FETs allowing a heavy load and requiring little space,
- Fig. 8 is a view similar to that of Fig. 3 of still another structure of interdigitated FETs allowing a heavy load and requiring little space, and
- Figs. 9a and 9b are views similar to Figs. 6a and 6b respectively illustrating a layout of FETs having well separated sources.

DETAILED DESCRIPTION

Field-effect transistors made for power amplifiers in e.g. mobile stations are commonly made by connecting a multitude of small or elementary FETs in parallel to produce a so called multifinger structure. An element finger 1 of such a FET is schematically illustrated in Fig. 2a as seen from above. The source 3 and drain 5 are seen as elongated rectangular parallel regions having their longitudinal directions in parallel to

each other and to the longitudinal direction of the gate region 7 located between the source and the drain. The gate region 7 is generally made of a metal layer on top of some electrically insulating layer. The signal is provided to the gate 7 as a voltage modulating the current between source and drain. The circuit diagram equivalent of the FET depicted in Fig. 2a is shown in Fig. 2b.

A dual band mobile station 9 communicating with base stations 11, 13 is illustrated in the schematic picture of Fig. 3. The antenna 15 of the mobile station is connected to receiver circuits 17 and through power FETs 19, 21 to transmitter signal processing circuits 23. The FETs are arranged in two groups A, B comprising the FET elements 19, 21, each FET element occupying an elongated rectangular area on a chip and each area being an elementary finger 1 as depicted in Fig. 2a. The FETs 19 of the first group A are intended to amplify signals for a lower wavelength and thus must be capable of providing a high output power and hence occupy a larger total area than the FETs 21 of the second group B intended for a higher wavelength band. This means, that if the elementary fingers of the two group of FETS have an equal length and thus occupy an equal area, the first FET needs more fingers than the second one. The first group A of FETs 19 thus comprises five fingers, the gates of the fingers being connected in parallel to one output terminal of the transmitter signal processing circuits 23, whereas the second group B of FETs 21 comprises a smaller number, in this case four fingers, the gates of the fingers being connected in parallel to another output terminal of the transmitter circuits 23. The total area of the FETs 19 of the first group A is physically or geometrically separated from the total area occupied by the FETs 21 of the second group. The layout of the fingers is shown in detail in the schematic view of Fig. 5a. In this figure it is seen that the antenna 15 is connected to the drains 5 of the elementary FETs of each group A, B and that the sources of the FETs of each group are connected in parallel, for instance to a common ground.

However, when the elementary FETs 19, 21 have to carry more load, such as when using more time slots in a time division multiplex system, each FET element will be more intensely heated and they must each be given more space on the chips, as is illustrated in Fig. 5b. The additional space requirement can be up to 50 - 100% of the space used in the layout illustrated in Fig. 5a. Since the transmission from the mobile station 9 always is on a single wavelength band, i.e. either on e.g. 900 MHz or 1900 MHz, and hence the FETs of each group are not simultaneously operated or energized, they can be interleaved so that most of the elementary FETs in an active group are separated by at least one elementary FET of the non-active group. Thereby the generated heat is distributed over a larger area and can be conducted away. Then most of the elementary FETs will have an effective space on the chip equal to twice the area of the element FET. Such a layout is illustrated in detail Fig. 5c and also appears from Fig. 4. Here each element FET of one group is located between element FETs of the other group, not considering the outermost FETs. The rectangular areas of each elementary finger are thus interleaved or interdigitated to

form a structure or pattern of rectangular regions placed with their long sides parallel to and at each other with a uniform spacing.

In the layout of the fingers as illustrated in Fig. 5a the drain of one finger is located directly at the side of the drain of the adjacent finger, so that the FET fingers are mirrored, i.e. every second finger of each group is identical, i.e. the 1st, 3rd and 5th fingers are identical to each other and the 2nd and 4th fingers are identical to each other in each group. In the embodiment the same configuration of having drains or sources in neighbouring transistors located directly at the side of each other is used. Every second finger is here identical, i.e. the 1st, 3rd, 5th, 7th, 9th fingers are identical to each other and constitutes the first group A of FETs and the 2nd, 4th, 8th, 10th fingers are identical to each other and constitutes the second group B of FETs.

In some cases it may be advantageous to locate the FETs of each group in pairs. Such a layout is illustrated in Fig. 6a. The outermost FETs thus belong to group A, the next two inner FETs belong to group B, the next two inner FETS to group A, etc. The circuit equivalent of the layout of Fig. 6a is shown in Fig. 6b.

Since the cooling of the chip can be better at the ends of the row or line of elementary FETs 19, 21, there can be more FETs of the group requiring a higher power at the ends. Such a structure is illustrated in Fig. 7. In the middle of the structure, as seen in a transverse direction, perpendicular to the long sides of the elementary regions 1, every second FET finger belongs to the first group A of FETs and every other second FET finger belongs to the second group B of FETs. More elementary FETs of the first group A, here a pair of FETs 19, are distributed at the ends of the structure as seen in the same direction, since, as has already been observer, at the ends the heat is more easily conducted away from the area.

Another embodiment is illustrated in Fig. 8. Here the fingers 19' of the first group A of FETs strictly alternates with fingers 21 of the second group B as in the embodiment of Fig. 4. In order to give the FETs of the first group a larger total area, the fingers 19' of this group are given a larger length than those of the second group of FETs 21. This embodiment apparently uses the area of the chip in a somewhat less efficient way than the embodiment of Figs. 5c, 6 and 7.

In some cases the sources of the different transistors cannot be placed directly at each other since such a location would cause a risk of cross-talk phenomena between the active and non-active transistor what could cause that also the non-active transistor would provide some output signal. Then the sources of the elementary transistors of the field effect transistors have to separated by a strip or gap having a suitable width, as is illustrated in Fig. 9a. The field effect transistors will then be completely electrically separated and the total area occupied by the field effect transistors will somewhat increased. The corresponding circuit diagram is shown in Fig. 9b.

CLAIMS

1. An amplifier circuit for amplifying signals, the circuit comprising at least two power field effect transistors, a first power field effect transistor and a second power field effect transistor different from the first power field effect transistor, the first power field effect transistor arranged to amplify first signals and the second power field effect transistor being arranged to amplify second signals, each power field transistor comprising a multitude of elementary transistors, the power field effect transistors and the elementary transistors having source, gate and drain electrodes, **characterized in** that the elementary transistors of the first power field effect transistor are located alternatingly with the elementary transistors of the second power field effect transistor, and that each elementary transistor comprised in the first power field effect transistor and located between two elementary transistors comprised in the second power field effect transistor has its source located directly at the source of the elementary transistor comprised in the second power field effect transistor and located at one side of the elementary transistor comprised in the first power field effect transistor and has its drain located at the drain of another elementary transistor comprised in the second power field effect transistor and located at a different side of the elementary transistor comprised in the first power field effect transistor.

2. An amplifier circuit according to claim 1, **characterized in** that it is arranged to amplify first and second signals, one of which is only present at each instant, so that when the first power field effect transistor is active the second power field transistor is inactive and vice versa, whereby elementary transistors of an active one of the power field effect transistors are separated by spaces in which elementary transistors of an inactive power field effect transistor are located.

3. An amplifier circuit according to any of claims 1 - 2, **characterized in** that is arranged for amplifying signals of at least two wavelength bands, the first signals being comprised in a wavelength band separate from a wavelength band, in which the second signals are comprised.

4. An amplifier circuit according to any of claims 1 - 3, **characterized in** that the elementary transistors occupy rectangular areas at the surface of a circuit plate, the rectangular areas have long opposite sides and short opposite sides, a long side of the rectangular area an elementary transistor located at a long side the rectangular area of another elementary transistor.

5. An amplifier circuit according to claim 4, **characterized in** that the rectangular areas of the elementary transistors of the first power field effect transistor and/or of the second power field effect transistor are identical to each other.

6. An amplifier circuit according to claim 4, **characterized in** that the rectangular areas of the elementary transistors of the first power field effect transistor are larger than the rectangular areas of the elementary transistors of the second power field effect transistor.

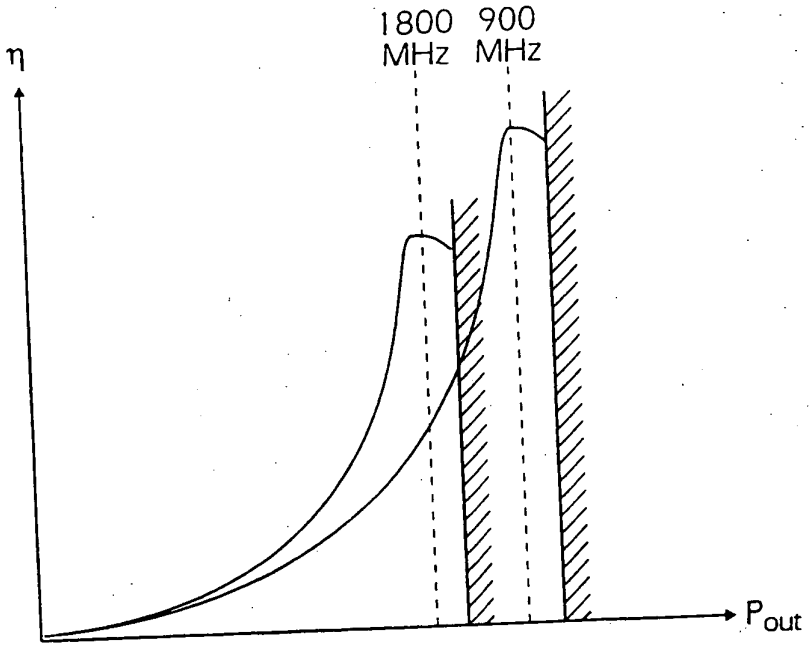


Fig. 1

Fig. 2a

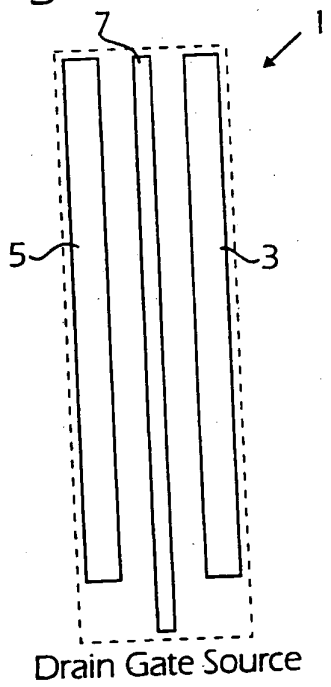


Fig. 2b

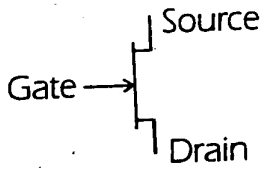


Fig. 3

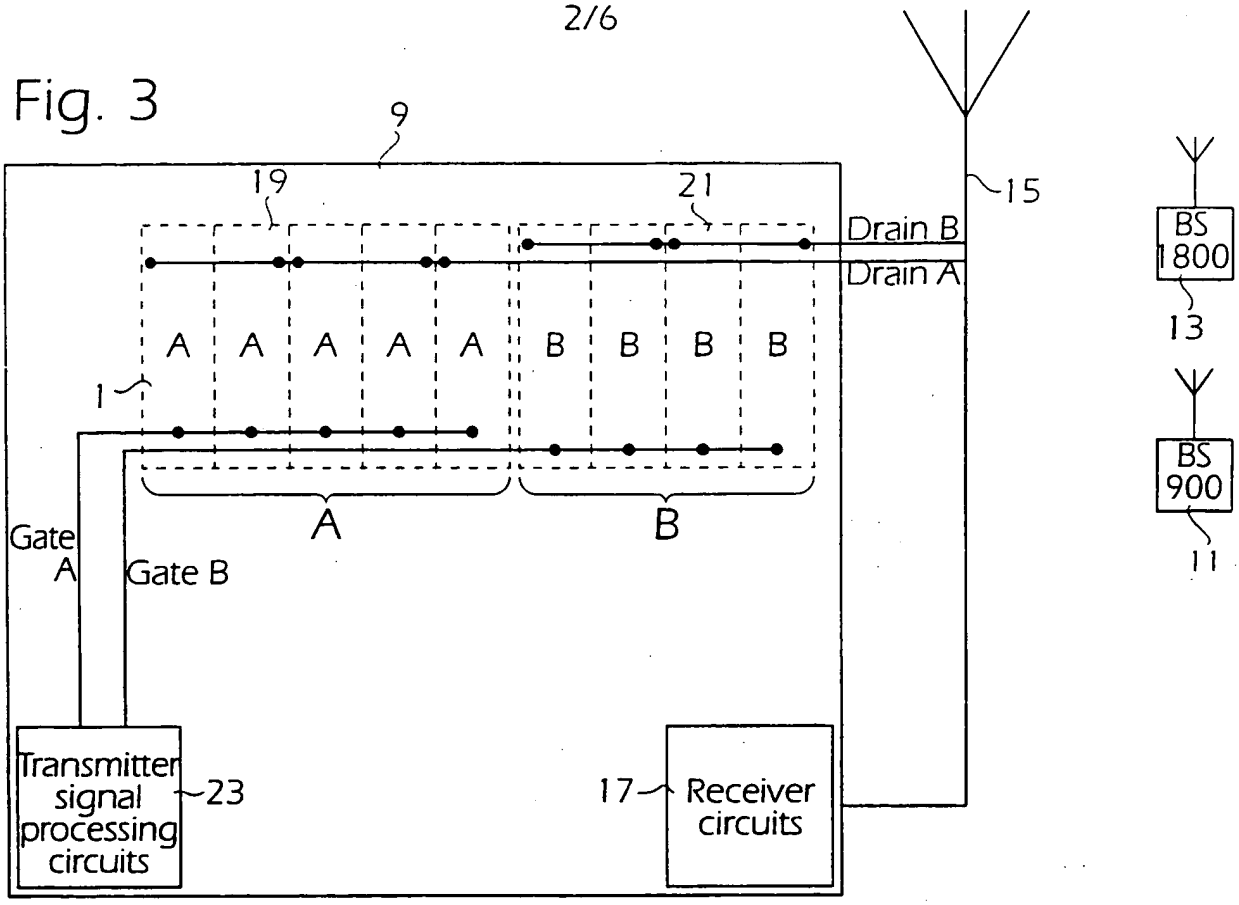
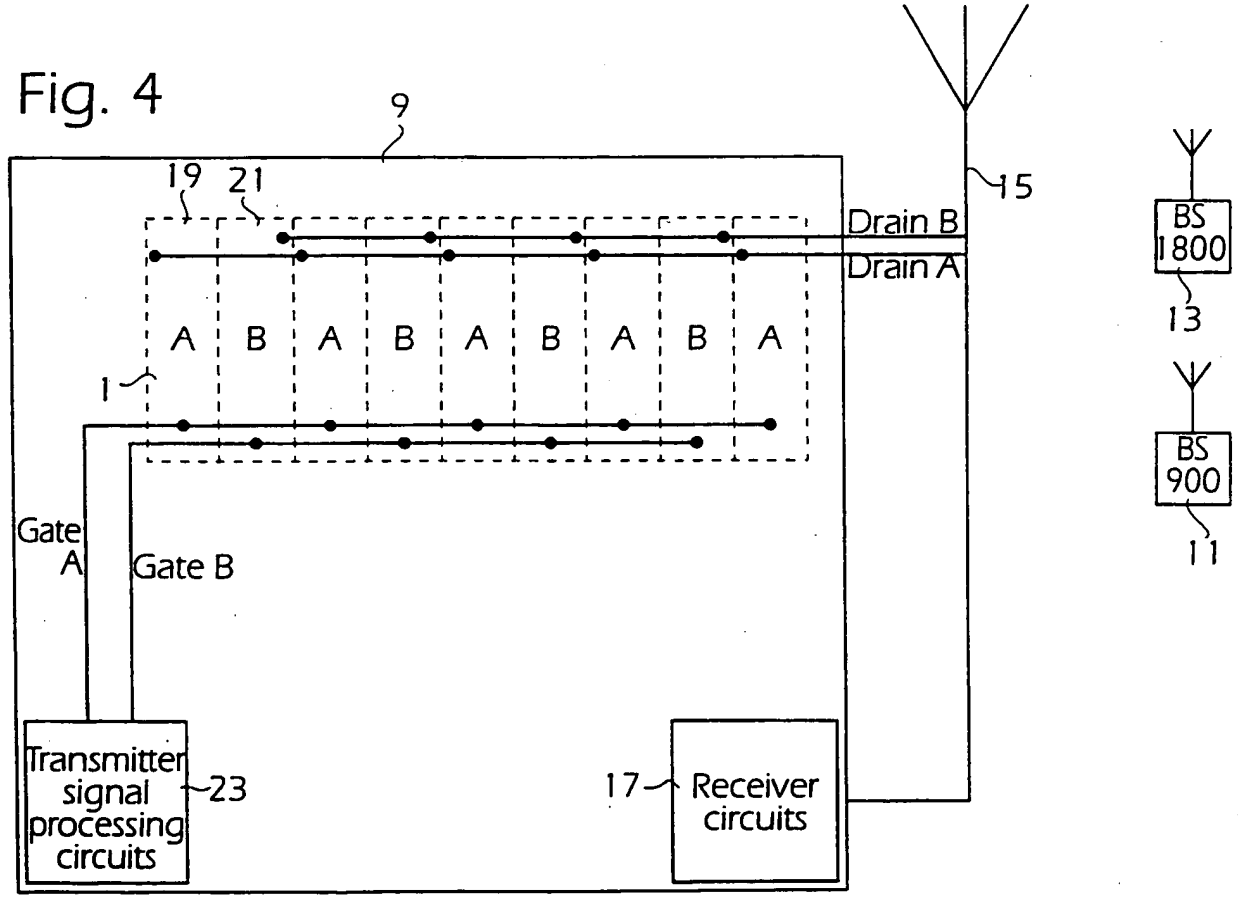

9
19
21
15
Drain B
Drain A
A A A A A B B B B
1
A
B
Gate A
Gate B
Transmitter signal processing circuits
23
17
Receiver circuits
BS 1800
13
BS 900
11

Fig. 4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Drain B
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Gate A
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Transmitter signal processing circuits
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Receiver circuits
BS 1800
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BS 900
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Fig. 5a

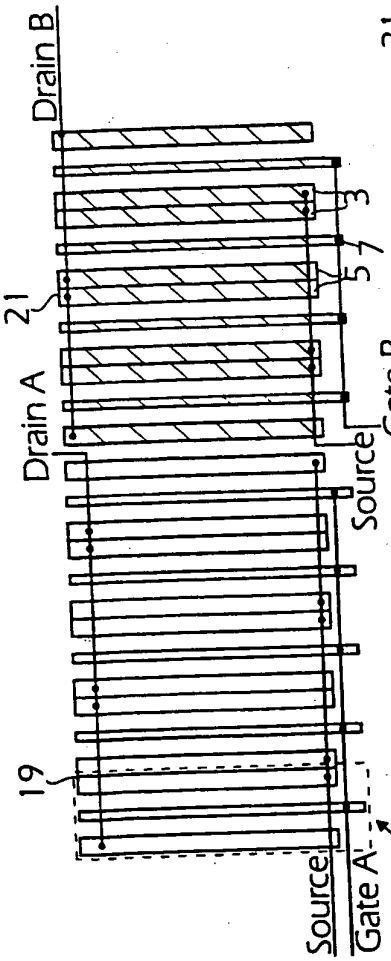


Fig. 5b

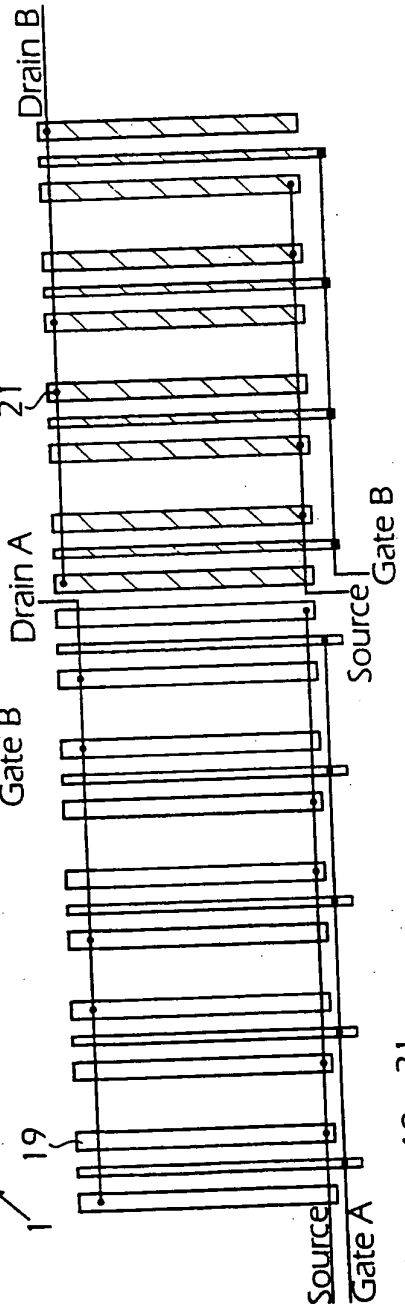
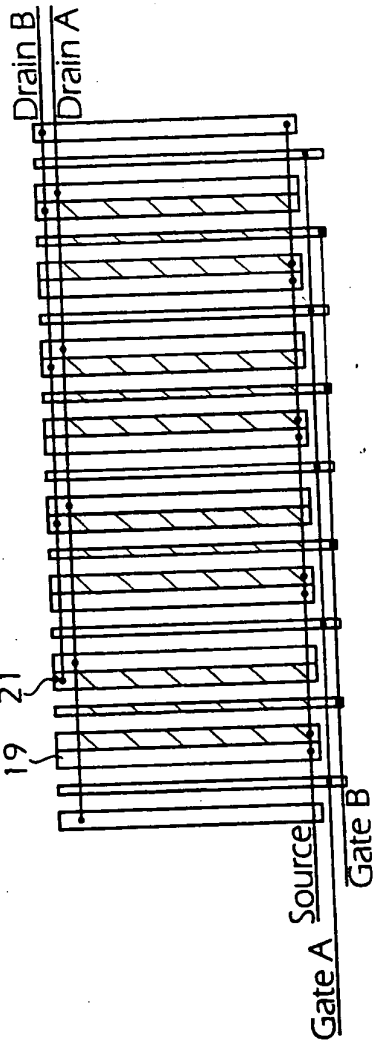
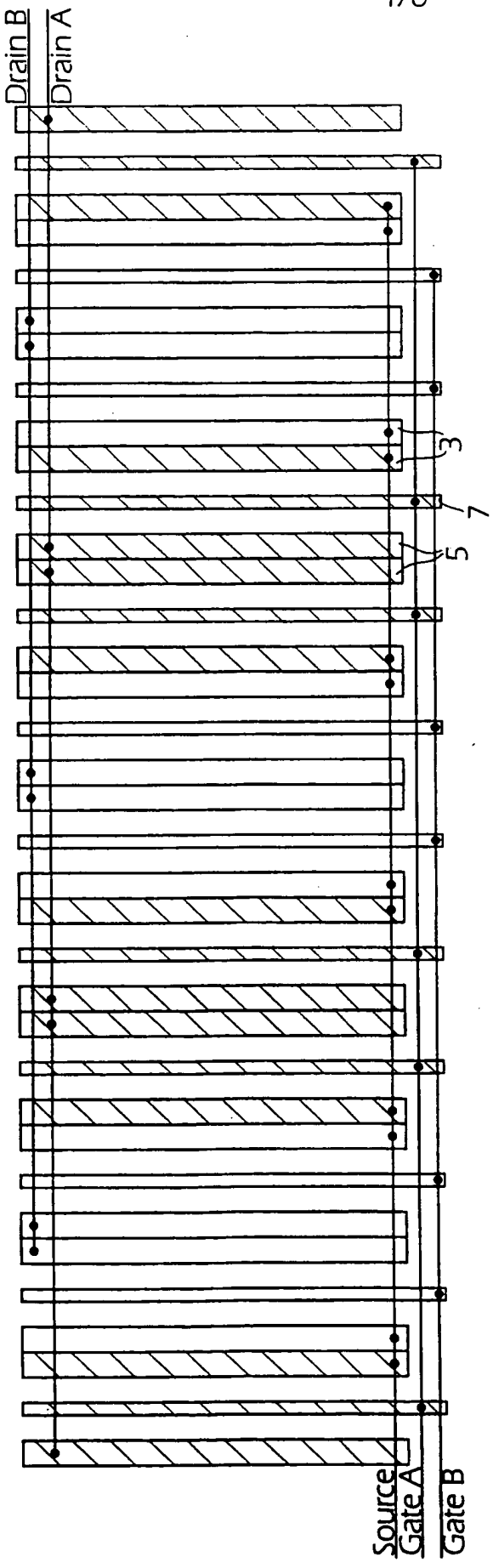


Fig. 5c

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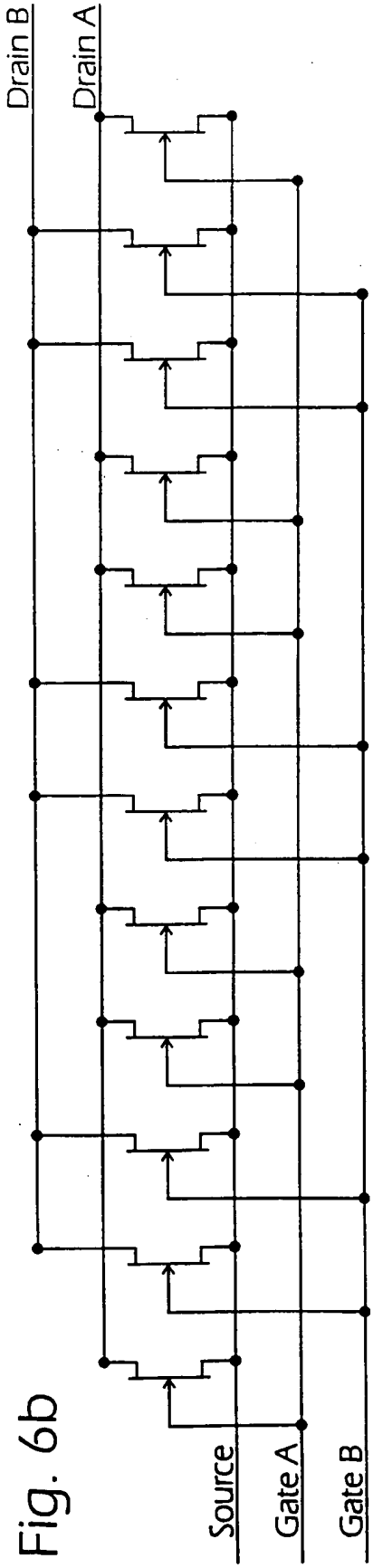
7
5
Source
Gate A
Gate B

Fig. 6a


Drain B
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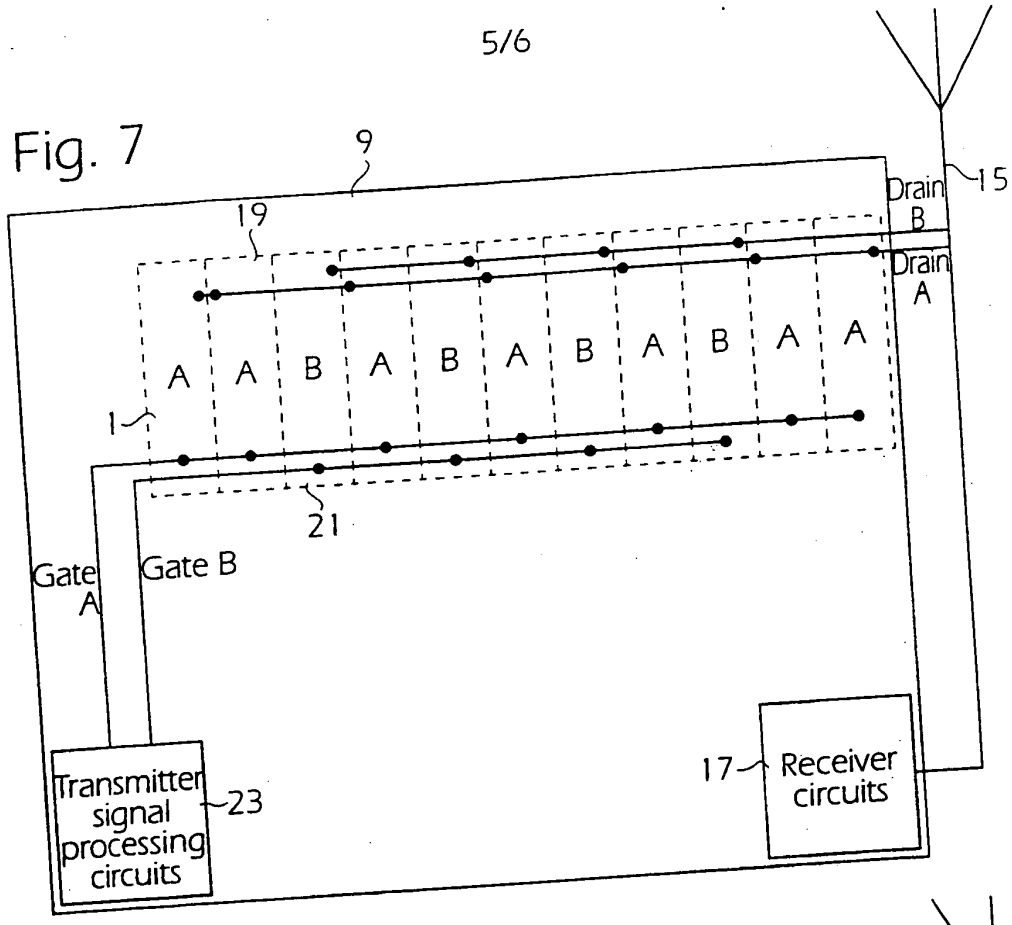
Source
Gate A
Gate B

Fig. 6b

Fig. 7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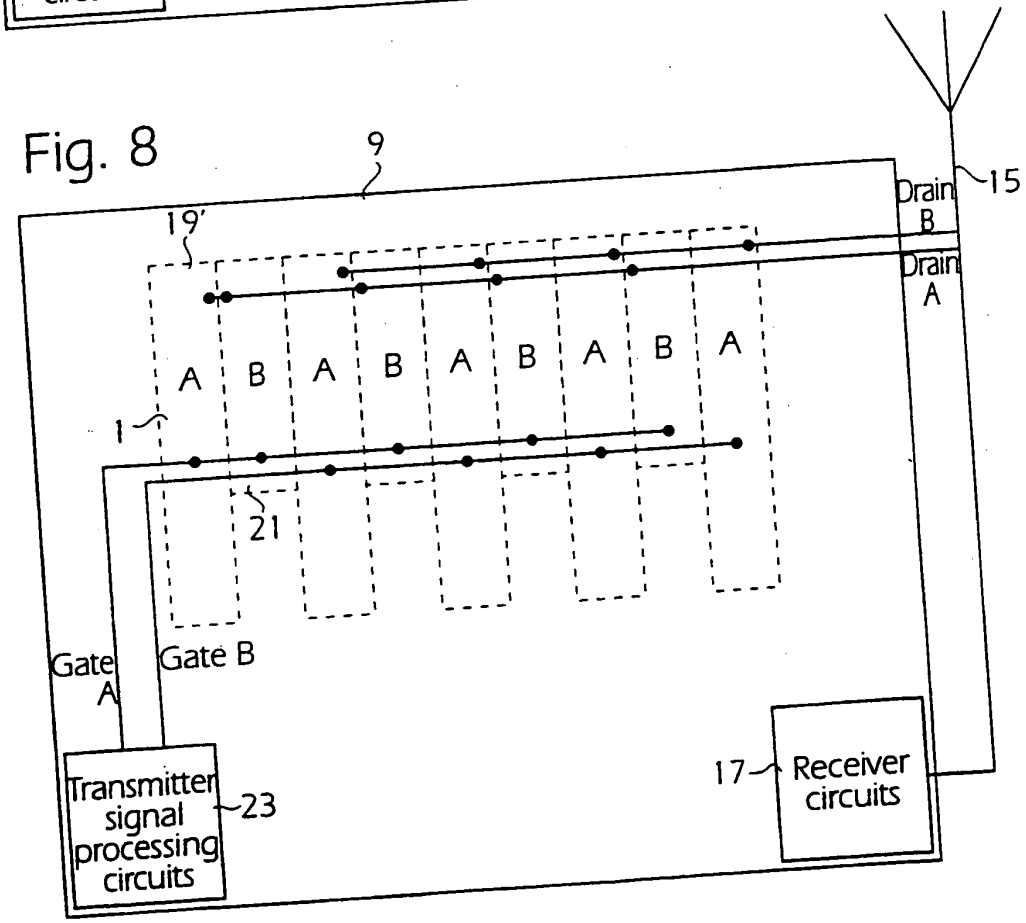
Gate A
Gate B
Transmitter signal processing circuits
23
17
Receiver circuits

Fig. 8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Transmitter signal processing circuits
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Receiver circuits

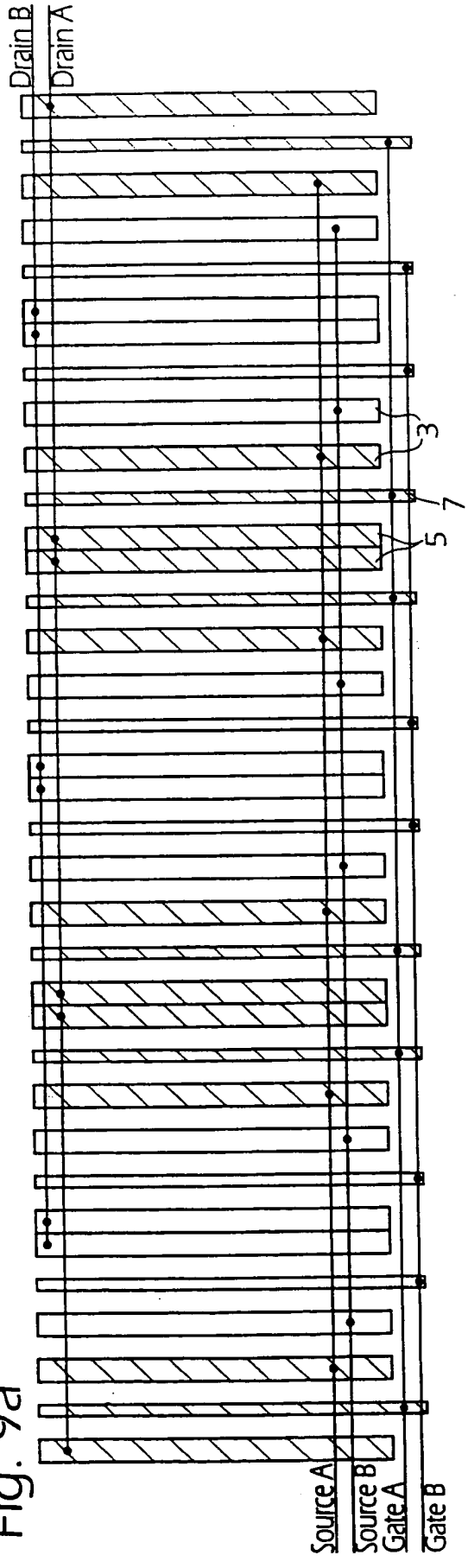

Fig. 9a

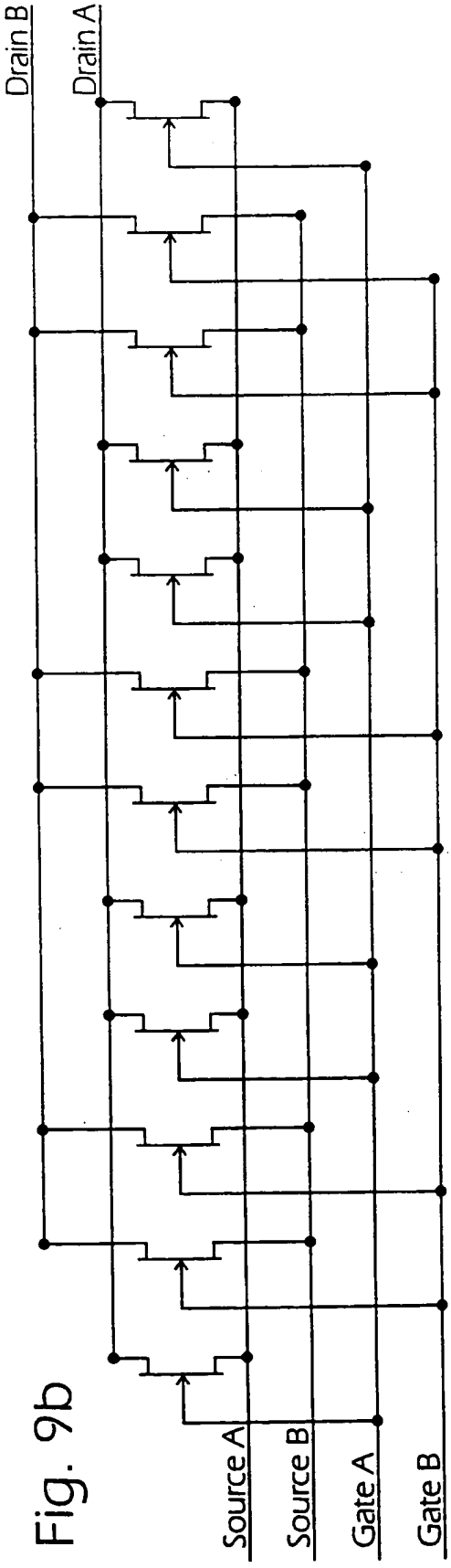

Fig. 9b

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 00/01882

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H01L 29/06, H01L 29/772, H03F 3/195
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H01L, H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4276516 A (JAMES S. CONGDON), 30 June 1981 (30.06.81), column 2, line 61 - column 3, line 14, figure 3a, abstract ---	1-6
X	US 4682197 A (FLAVIO VILLA ET AL), 21 July 1987 (21.07.87), column 3, line 41 - column 4, line 7, figure 3, abstract ---	1-6

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
29 January 2001	02 -02- 2001
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Birgit Politt/MN Telephone No. +46 8 782 25 00

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INTERNATIONAL SEARCH REPORT

Information on patent family members

27/12/00

International application No.
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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